Nanotechnology in Electron Devices

Bob Gasser
Vice President
Director, Components Research
Intel Corporation

intel

Outline

- Key Messages
- What is Nanotechnology?
- Microtech and Nanotech History
- Nanotech State of the Art
- The Future
- The Ultimate Vision
- Summary
- Q+A

Key Messages

- Nanotechnology is here today in "state of the art" high speed Si CMOS process technologies
- Si nanotechnology process scaling/convergence will continue for the next 10-15 years
- Alternative new technologies have emerged and will begin to be integrated into Si CMOS by 2015
- Nanoscience research is needed to facilitate these radical new scalable technologies beyond 2020

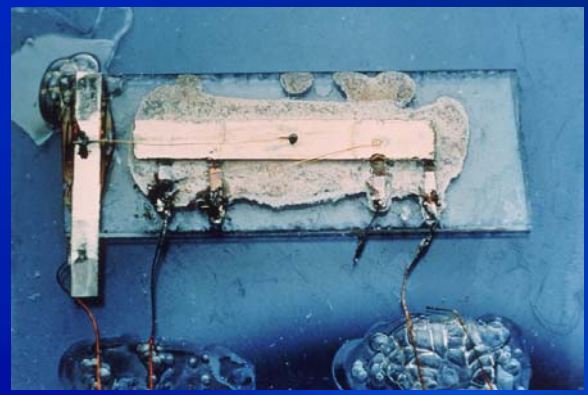
intel

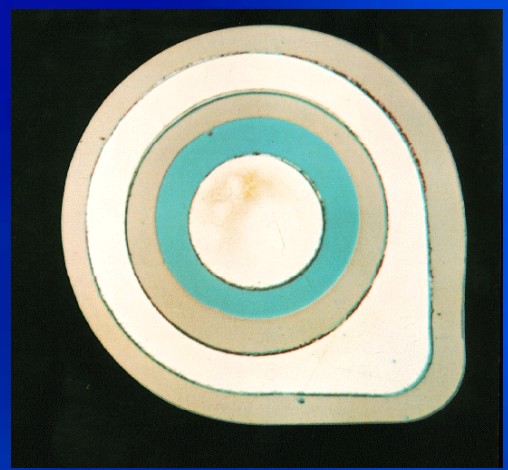
What is Nanotechnology?

a. New structures like carbon nanotubes
b. Silicon devices made smaller
c. Arranging atoms and molecules
d. Letting atoms assemble themselves
e. Something far in the future
f. In production today
g. All of the above

Microelectronics and Nanotechnology History

- 1959
  - First Germanium Hybrid Integrated Circuit and First Silicon Planar Integrated Circuit Demonstrated.
    - Jack Kilby, Robert Noyce
- 1959
  - "Plenty of Room at the Bottom"
    - Richard Feynman
    - http://www.zyvex.com/nanotech/feynman.html





intel

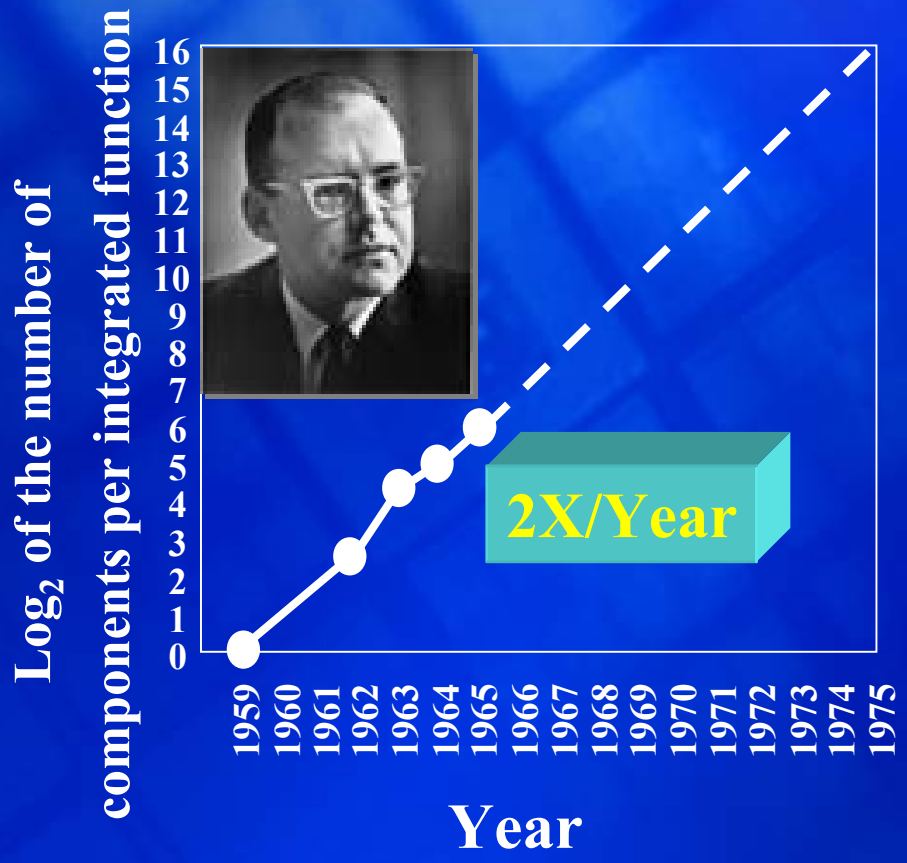
Vision of Nanotechnology in 1959

The Principles of Physics, as far as I can see, do not speak against the possibility of Maneuvering things atom by atom. It is not an Attempt to violate any laws; it is something, in Principle, that can be done; but in practice, it Has not been done because we are too big"

Richard Feynman

intel

Birth of Microelectronics: Moore's Law



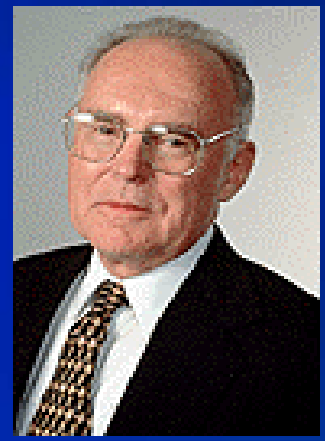
"Reduced cost is one
Of the big attractions of
Integrated electronics, and
The cost advantage continues
To increase as the technology
Evolves toward the production
Of larger and larger circuit
Functions on a single
semiconductor substrate."

"Dr.Gordon E.Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather then in electronics."

Electronics Magazine (35th anniversary), April 19, 1965

intel

I see no reason to expect the rate of progress
In the use of smaller dimensions in complex
Circuits to decrease in the near future.



With respect to the factor contributed by Device and Circuit
Cleverness, however, the situation is different.
We are approaching a limit that must slow the rate of progress

Gordon Moore, IEDM 1975

Micro and Nano History 1

- **1974**
  - ***Norio Taniguchi invents the word "Nanotechnology" to signify the construction of machines with tolerances less than one micron***
- **1979**
  - **The Semiconductor Industry reaches the $10 Billion mark**
  - **3-year cycle established**
- **1981**
  - ***Scanning tunneling microscope (STM)***
    - ***Heinrich Rohler and Gerd Karl Binning.***

intel

Micro and Nano History 2

- **1981**
  - **IBM, Intel, Microsoft enter the personal PC**
- **1985**
  - ***Buckyballs discovered***
    - ***Richard Smalley, Robert Curl, Jr., Harold Kroto***
- **1985**
  - ***Yoshida Nano-Mechanics is launched in Japan***
- **1986**
  - **1 Micron CMOS Technology goes into high volume manufacturing**

intel

Micro and Nano History 3

- **1986**
  - *Atomic Force Microscope (AFM)*
- **1986**
  - *Publication of "Engines of Creation". A vision of molecular nanotechnology*
    - *K.Eric Drexel.*
    - *http://www.foresight.org/EOC/Engines.pdf*
- **1987**
  - *First Single-Electron Transistor demonstrated*
    - *Theodore A. Fulton and Gerald J. Dolan*

Micro and Nano History 4

- **1990**
  - **The Semiconductor Industry reaches $50B**
- **1991**
  - ***Carbon Nanotube discovered as part of ERATO program in Japan (1981-2001)***
    - ***Sumio Ijima***
- **1994**
  - **The Semiconductor Industry reaches $100B**

Micro and Nano History 5

- **1995**
  - **The Semiconductor Industry accelerates to 2-year cycle**
- **1997**
  - ***DNA-based nanomechanical devices created***
    - ***Nadrian Seeman***
- **1999**
  - ***Electronic Molecular Switch created***
    - ***Mark Reed and James M. Tour***

Micro and Nano History 6

- **2000**
  - **The Semiconductor Industry passes the $200B mark**
  - **30nm CMOS demonstrated**
- **2000**
  - ***Sub-100nm transistors in volume production***
- **2001**
  - ***Nanotube logic demonstrated with carbon nanotubes***

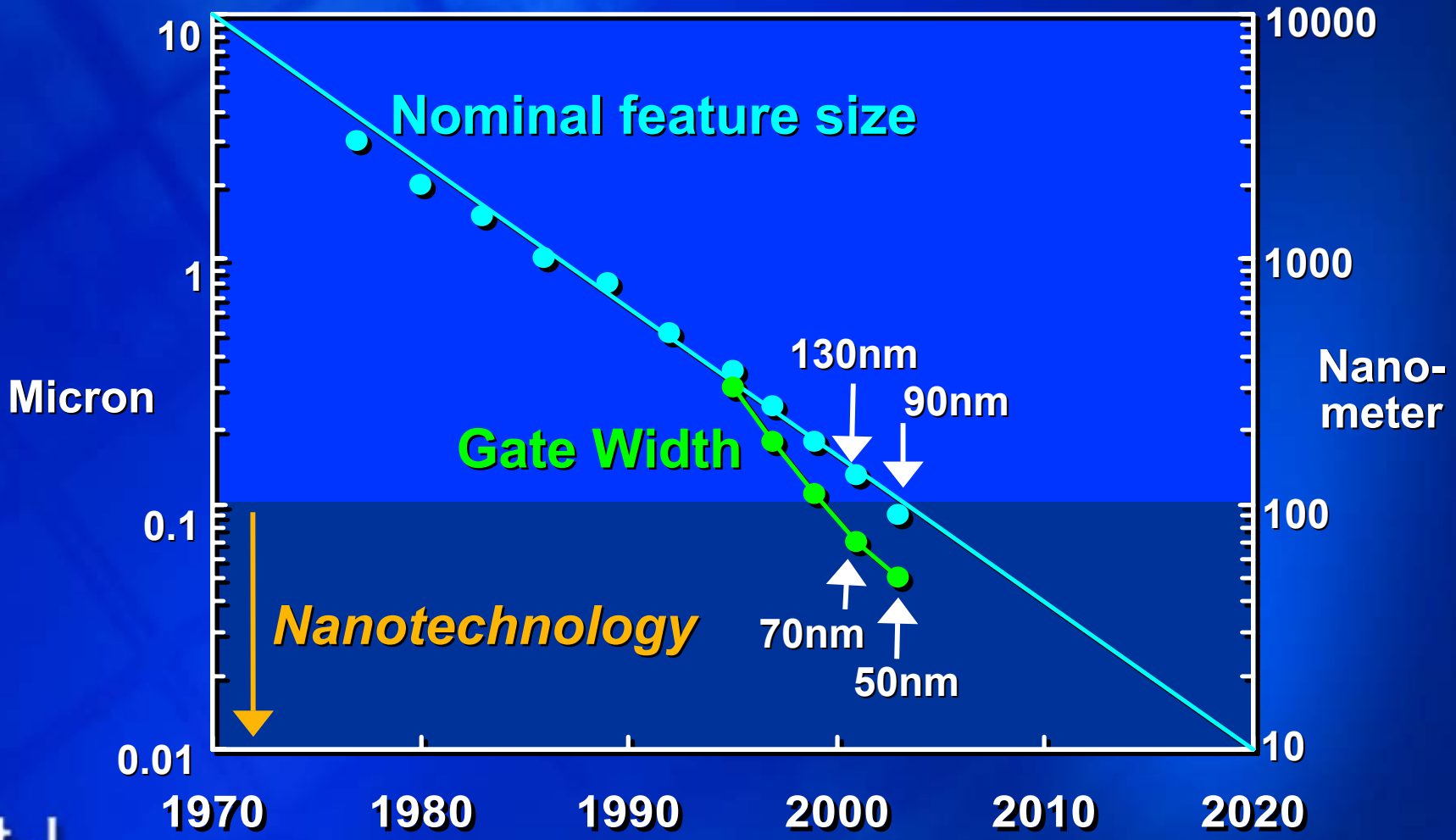
intel

NSET* Nanotechnology Definition (Feb 2000)

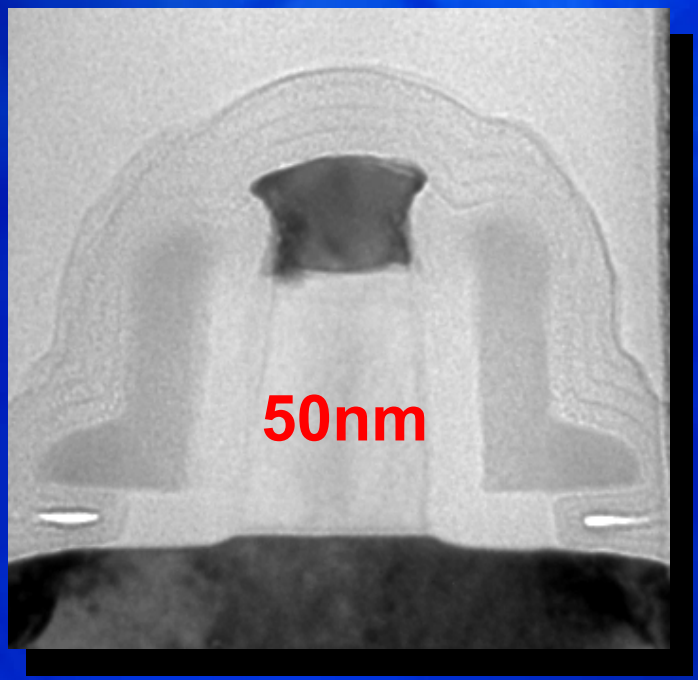
Research and technology development at the atomic, molecular, or macromolecular levels, in the length scale of approximately 1 – 100 nanometer range

*National Science and Engineering Technology Council

Silicon Nanotechnology is Here!

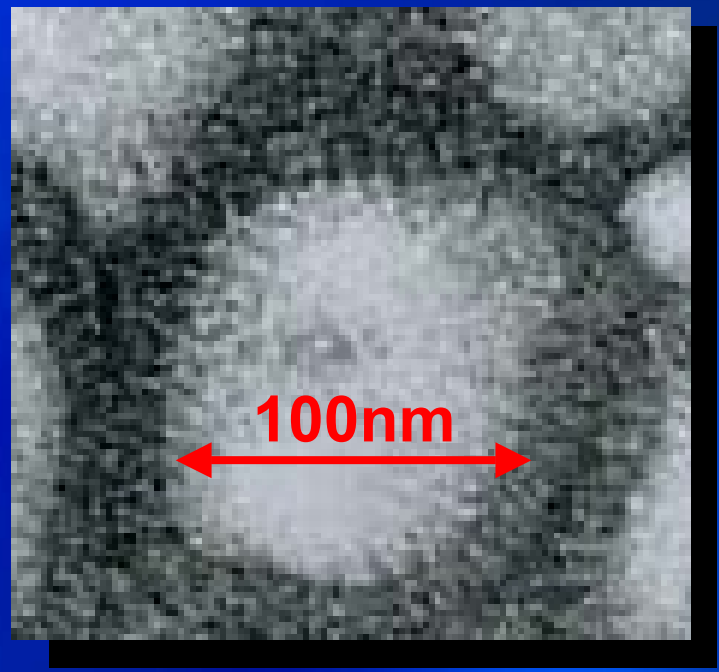


Silicon Devices Shrink to Virus Size



Transistor for 90nm Process

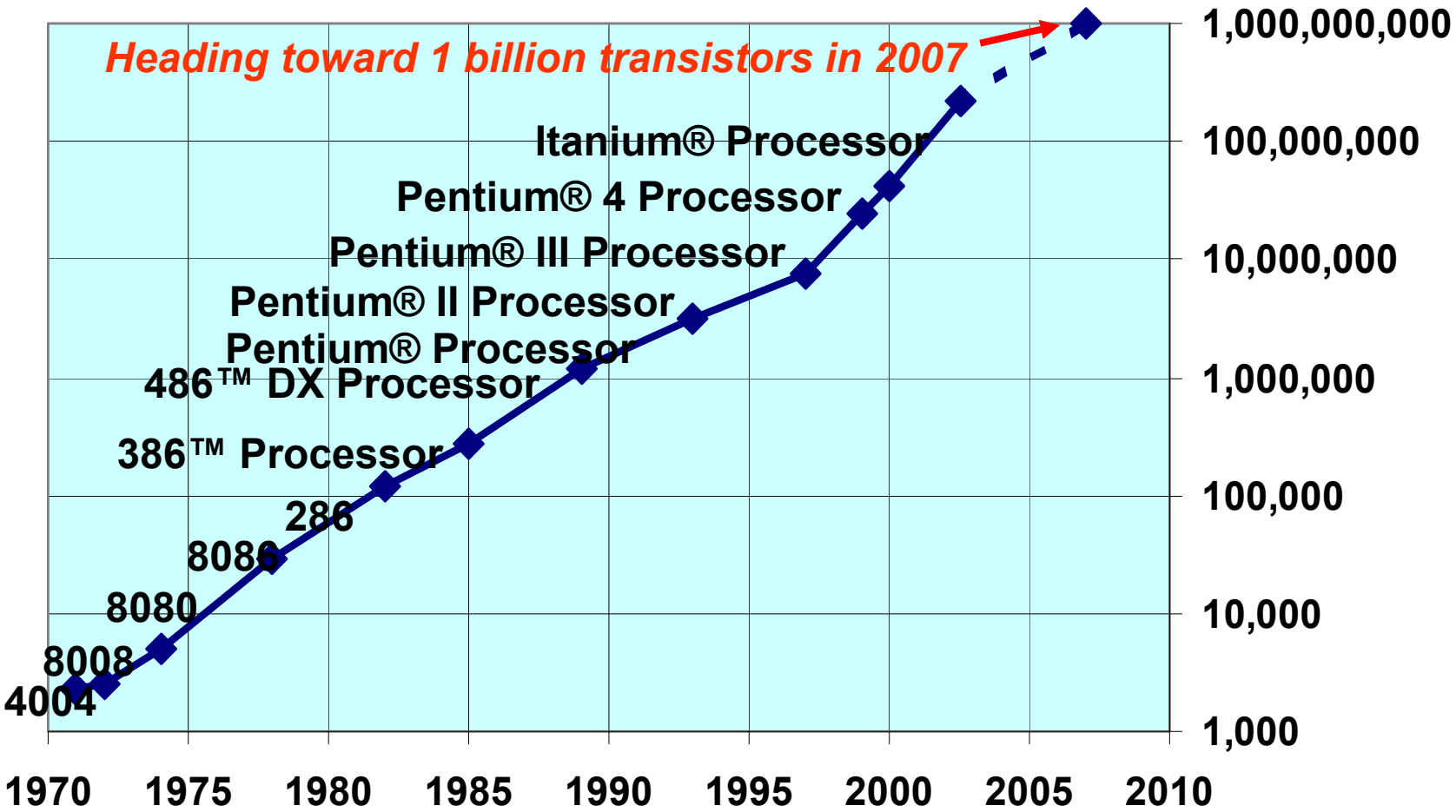
Source: Intel



Influenza virus

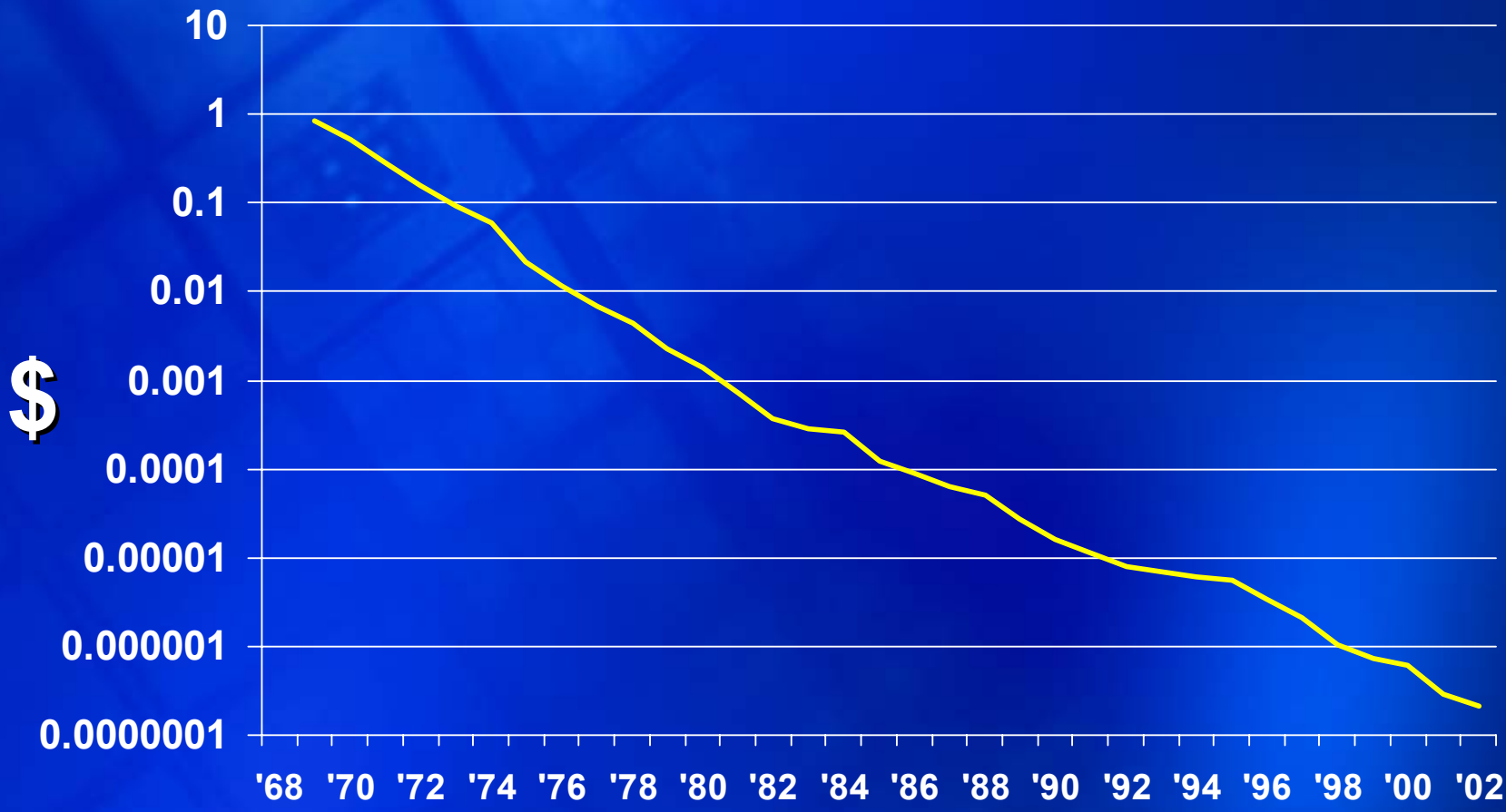
Source: CDC

Moore's Law In Action



>220M Transistors Integrated Into Devices Produced Today

>6 Orders Of Magnitude Reduction in Cost/Transistor



Source: WSTS/Dataquest/Intel, 8/02

New Materials, Devices Extend Si Scaling

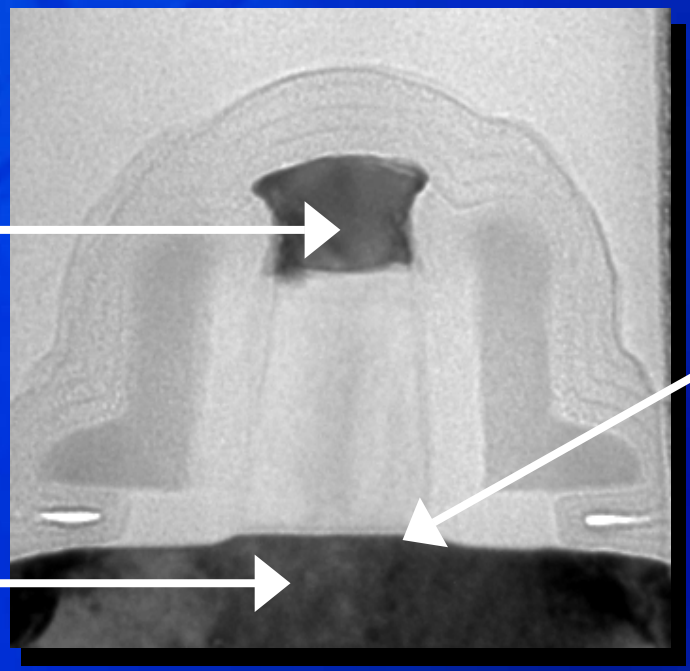
Changes Made

Gate

Silicide added

Channel

Strained silicon



Transistor

Future Options

High-k gate dielectric

New transistor structure

Source: Intel

New Materials, Devices Extend Si Scaling

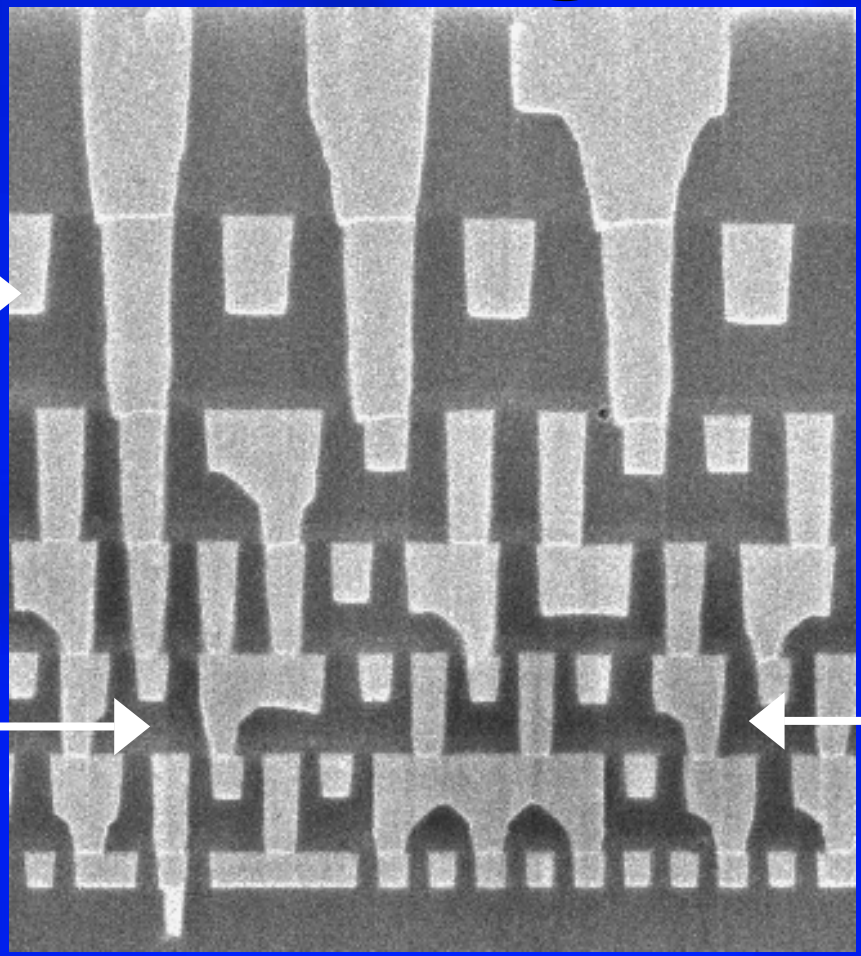
Changes Made

Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF → CDO (low-k)



Interconnects

Source: Intel

Future Options

Ultra Low-k Dielectric

The Future

- **Continue CMOS Nanoscaling**
- **Non-classical CMOS**
- **Convergence**
- **Novel devices**

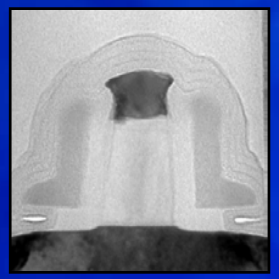
Nanotechnology features

- Structures measured in nanometers
  - Less than 0.1-micron (100nm)
- New materials and device structures
  - Incrementally changing silicon technology base
- Materials manipulated on atomic scale
  - In one or more dimensions
- Increasing use of self-assembly
  - Using chemical properties to form structures

intel

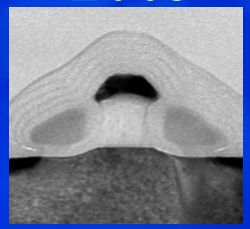
Intel Nano Transistors

90nm Node
2003



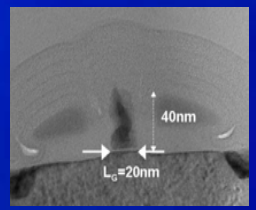
50nm Length
(IEDM2002)

65nm Node
2005



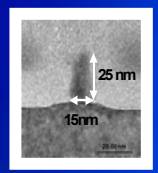
30nm Prototype
(IEDM2000)

45nm Node
2007



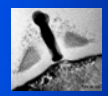
20nm Prototype
(VLSI2001)

32nm Node
2009



15nm Prototype
(IEDM2001)

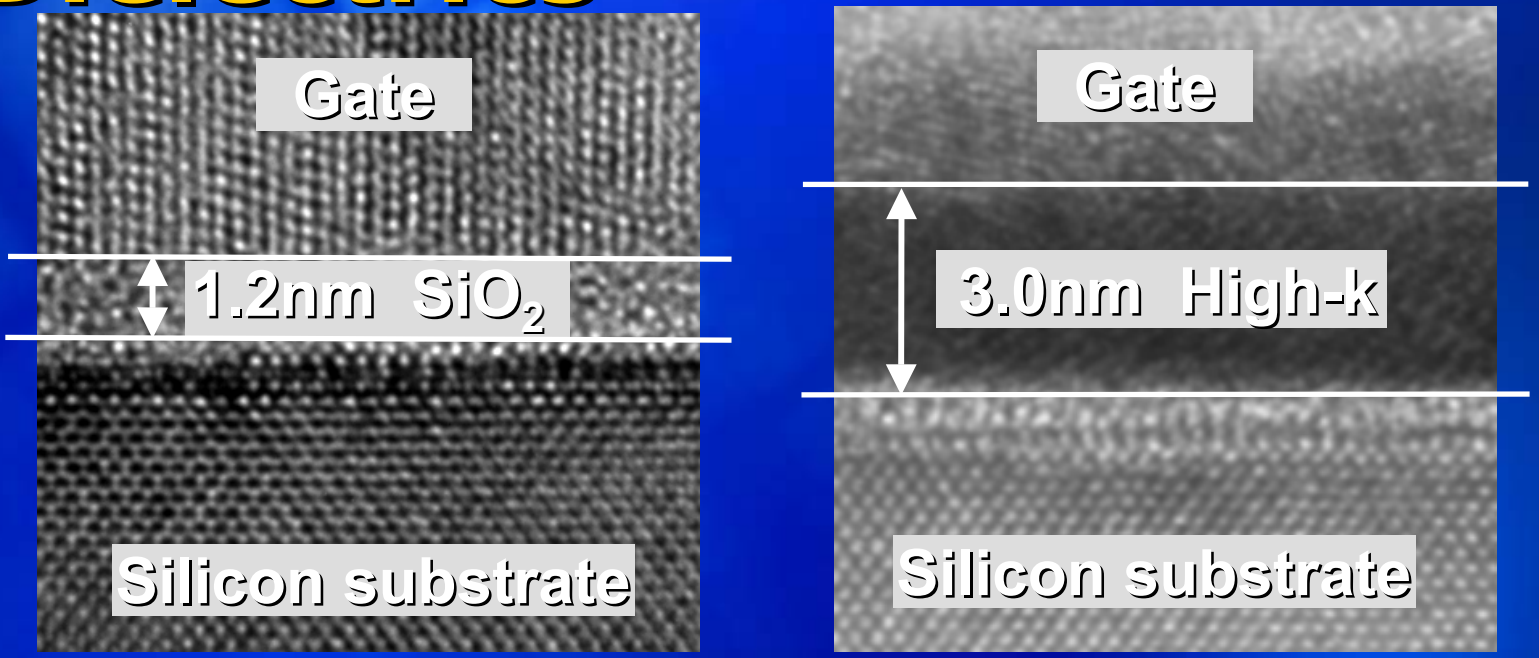
22nm Node
2011



10nm Prototype
(ITJ 2002)

Increasing leakage

Nanotechnology for Gate Dielectrics



Source: Intel

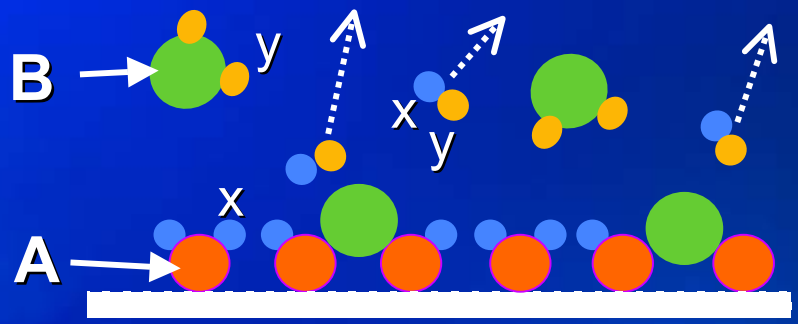
	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Integration is the key challenge

Crafting Films with Atomic Layer Deposition

Step 1

Step 2



Step 3

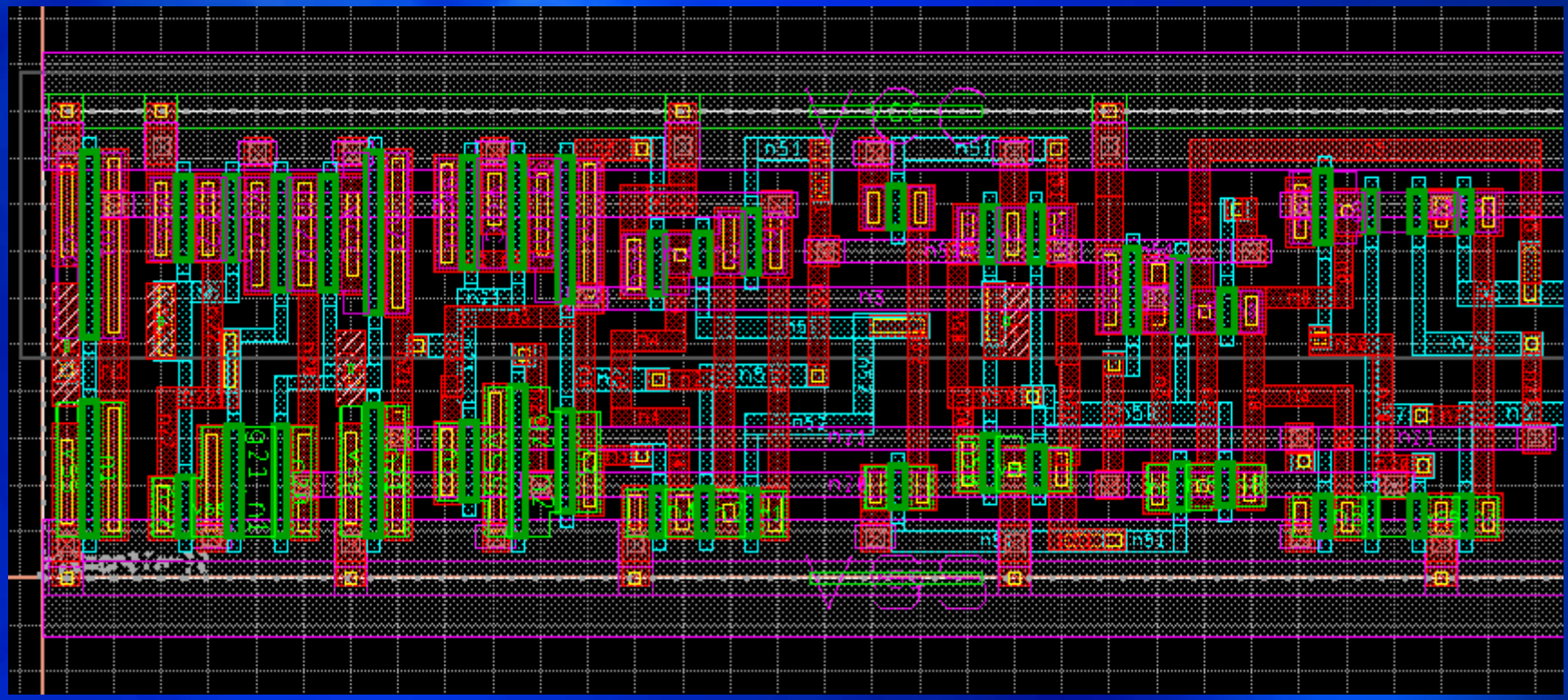
Step 4

ALD: Today's nanotechnology for self-assembly by atomic layer

intel

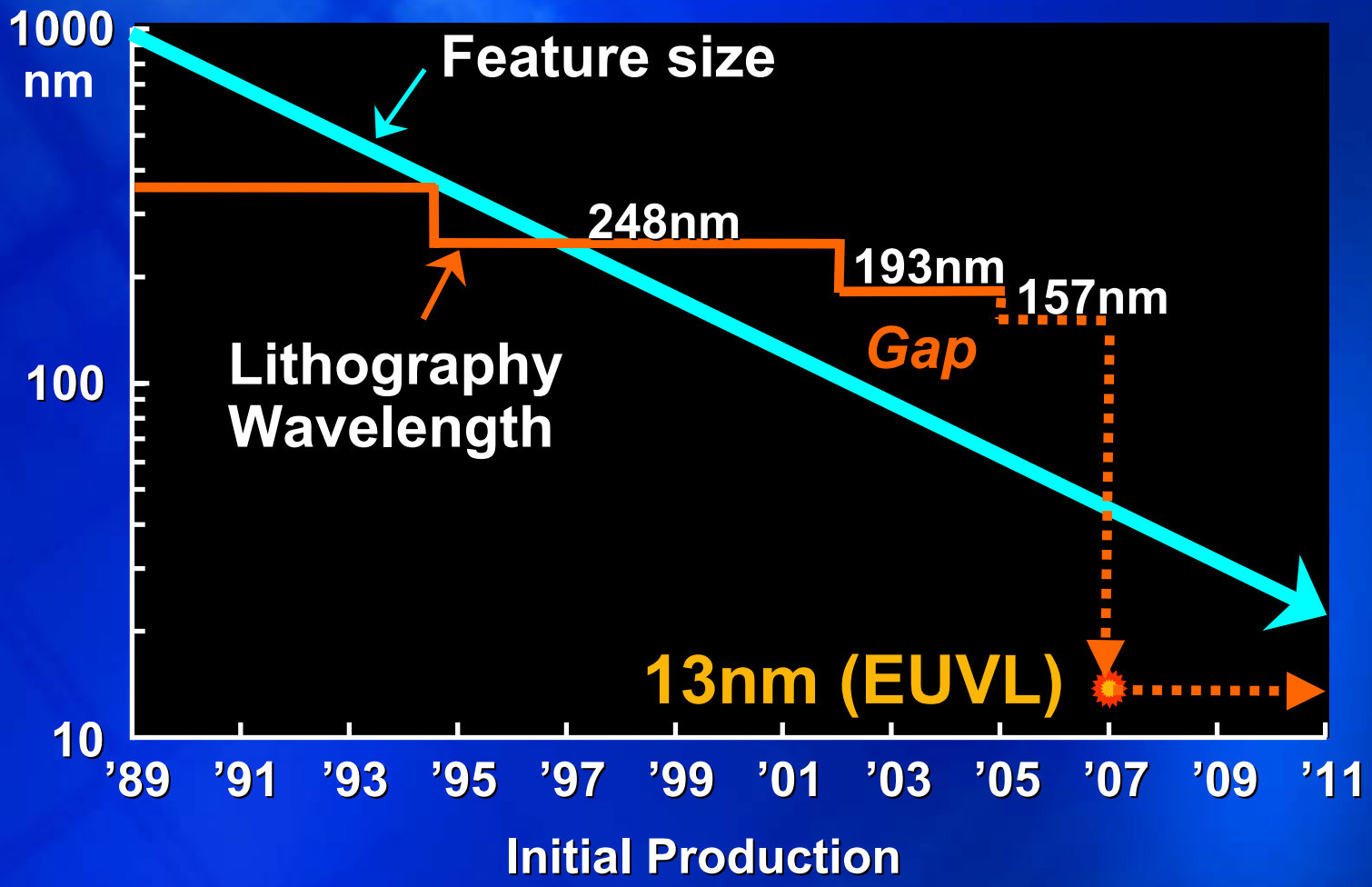
26

Lithography is the Designer's "Brush"

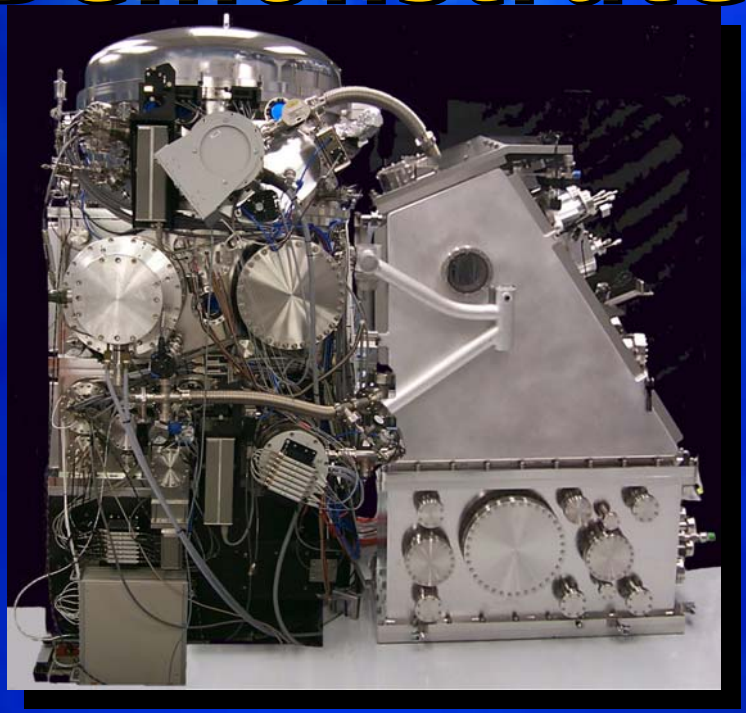


Lithography is indispensable for defining locations/configurations of circuit elements/functions

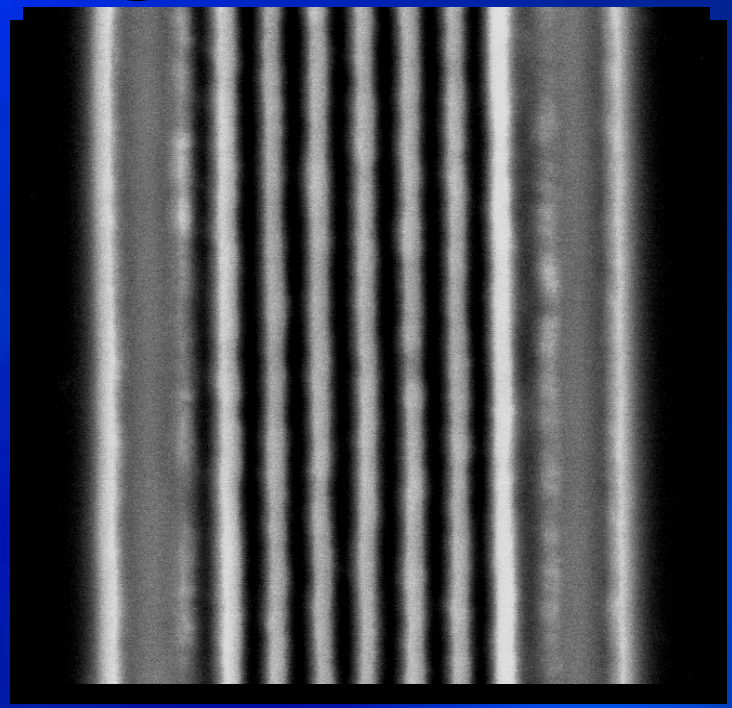
Lithography Gap to Close with EUVL



EUV LLC Consortium Demonstrates EUVL



EUV Lithography Prototype Exposure Tool



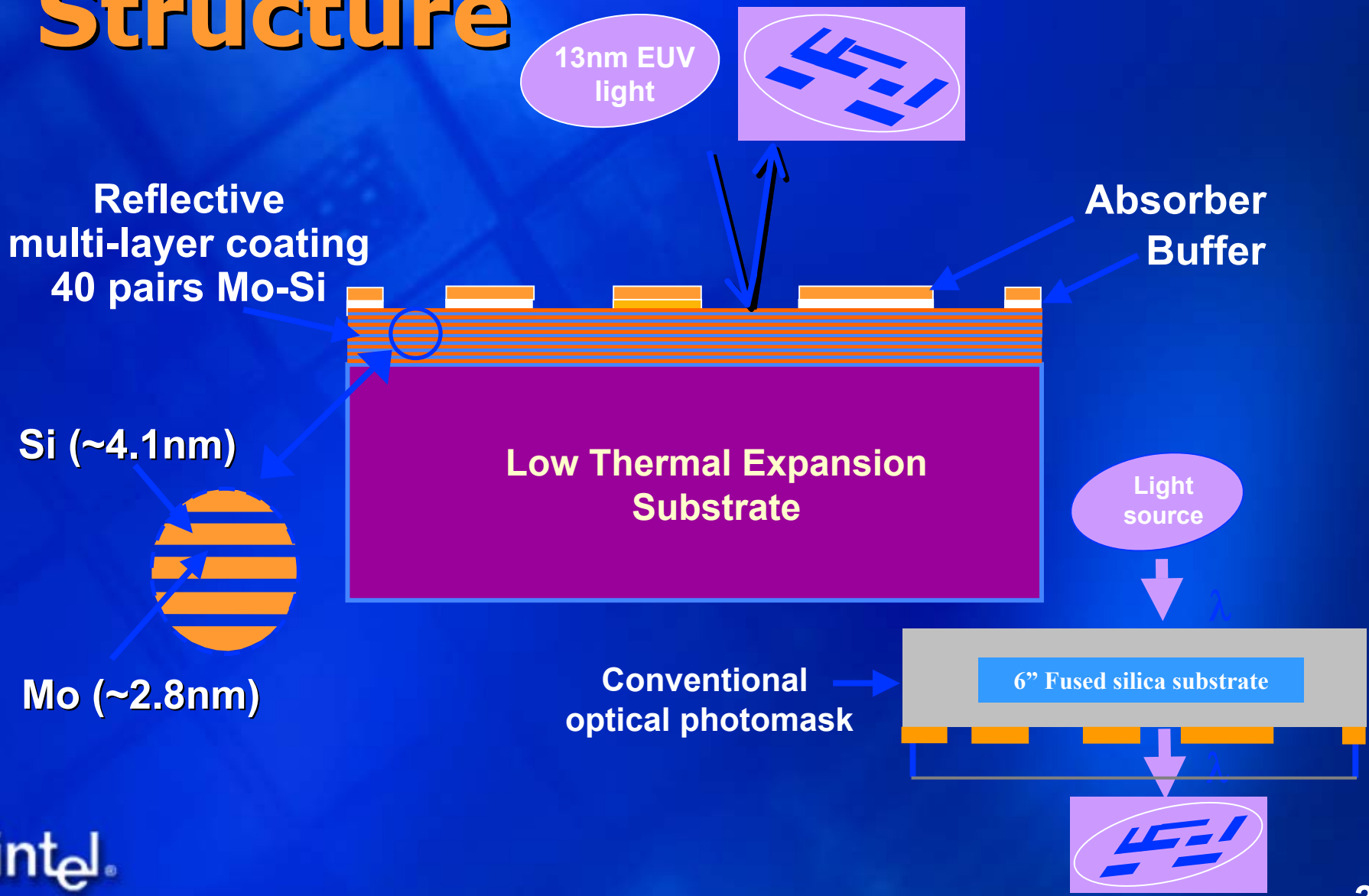
50nm Lines Printed with EUV Lithography

Source: Sandia

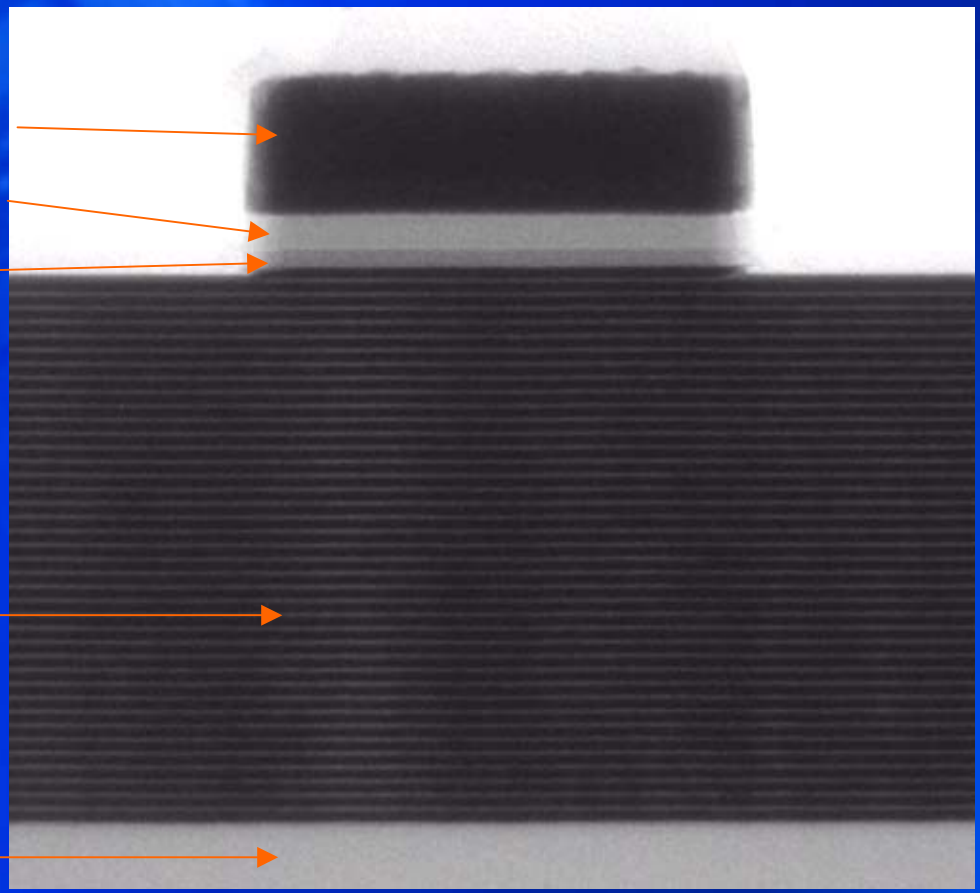
EUV lithography is now in commercialization phase

intel

EUV Reflective Mask Structure



Cross Section of a Fully Fabricated EUV Mask



R = 67%
3σ = 0.5%
@ 13.4nm

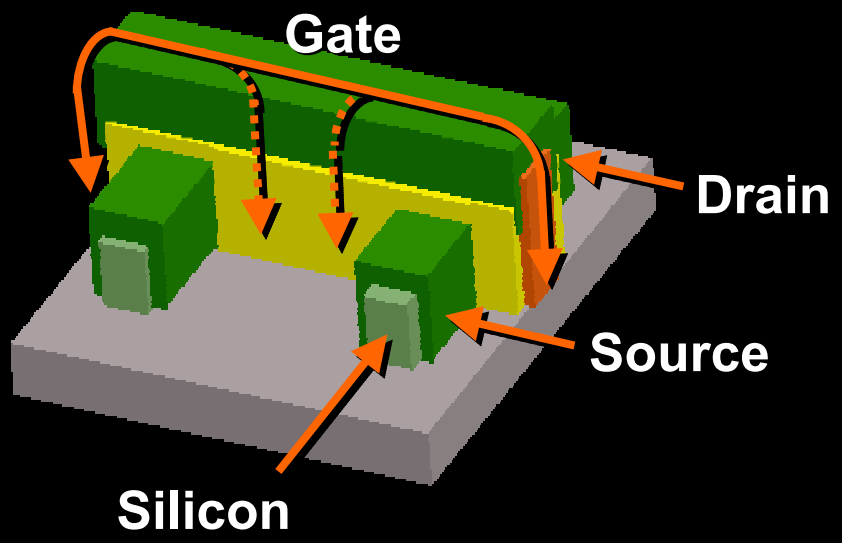
Excellent absorber patterning!

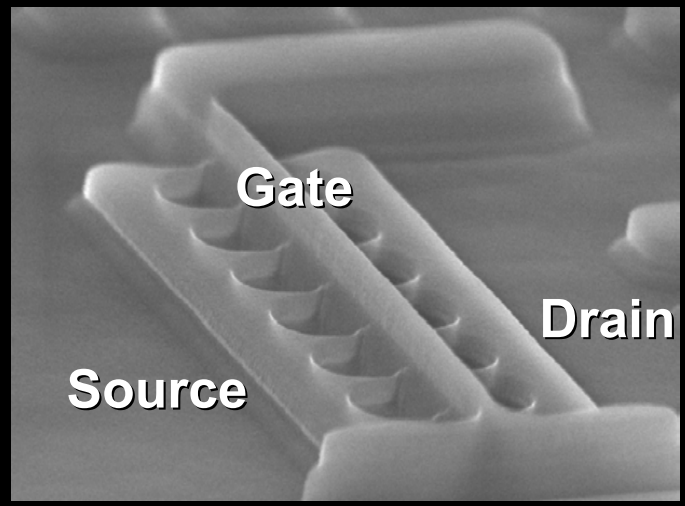
intel

The Future

- Continue CMOS Nanoscaling
- Non-classical CMOS
- Convergence
- Novel devices

Experimental Tri-Gate Transistor





Source: Intel

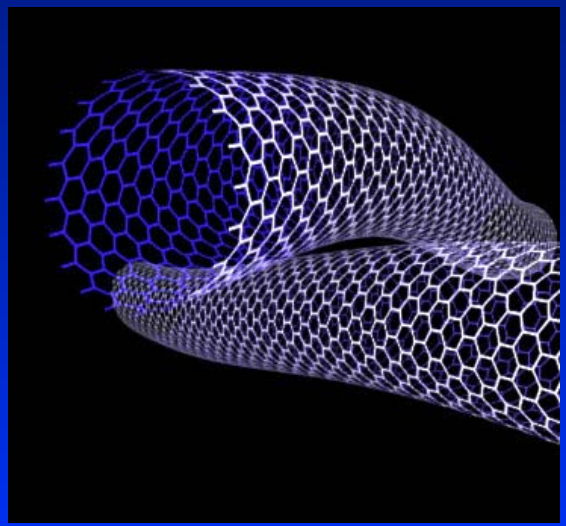
- **Improved version of TeraHertz transistor**
  - **Better performance**
  - **Scalable to smaller sizes (low leakage)**
  - **Possible intercept towards end of decade?**

intel

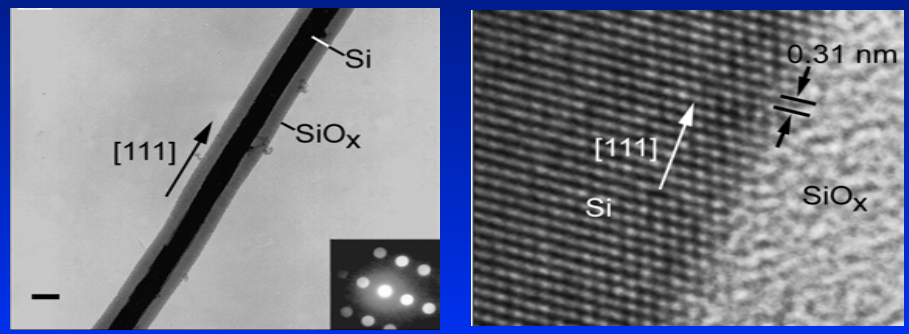
Nanotubes/Nanowires (>> 2010?)

- Collaborations with universities in progress
- Good individual device data, many integration and materials issues to be resolved

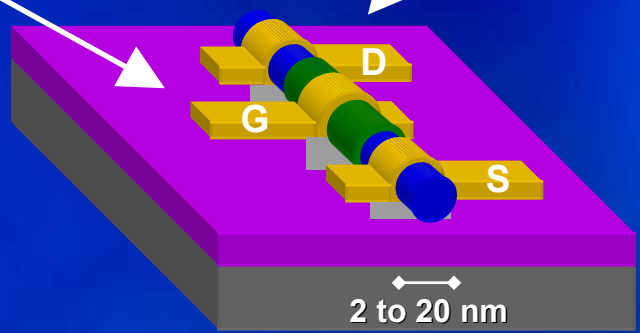
Carbon Nanotube



Silicon Nanowire



Source: Morales & Lieber, Science **279**, 208 (1998)



The Limits of Logic Scaling

- For an *arbitrary* switching device made of of a single electron in a dual quantum well
  - Operating at room temperature
- It can be shown a power dissipation limit of 200 W/cm**2
- Will limit the operational frequency to ~100 GHz at length scales ~ 4 nm

The Future

- Continue CMOS Nanoscaling
- Non-classical CMOS
- Convergence
- Novel devices

Marriage of High Speed Logic with Other Technologies

- Flash/DRAM
- RF

{ Today

- MEMS/NEMS
- Optoelectronics
- Bioelectronics
- Alternate memory
  - MRAM, FeRAM, Ovonics

{ Future

intel

Intelligent Silicon

Nano is Here

New Devices,
Materials, and Processes

Expanding the Silicon Canvas

EXPANDING

Sensors

Optical

Nano

Wireless

Mechanical

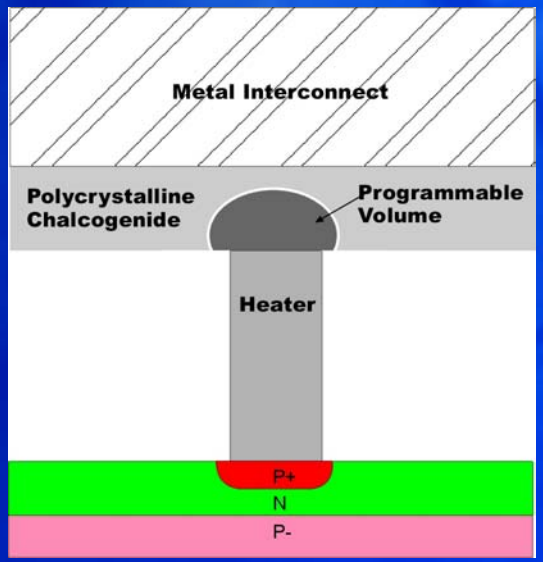
EXTENDING MOORE'S LAW

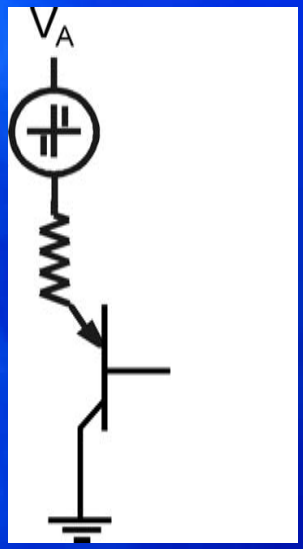
Discrete SSI LSI VLS

Silicon Innovation Enabling Convergence

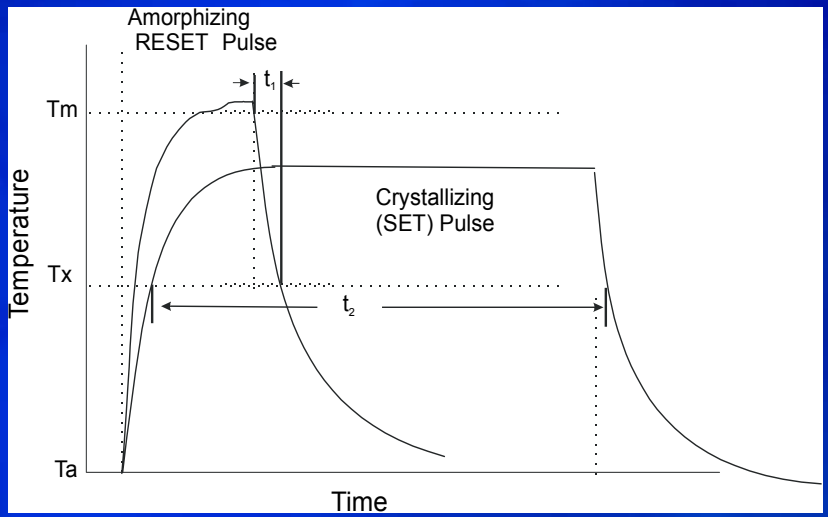
intel

Ovonics Unified Memory





- **Operation**
  - Chalcogenide mtl alloys used in re-writable CD's and DVD's
  - Electrical energy (heat) converts between crystalline and amorph.
  - Cell reads by measuring resistance



- **Attributes**
  - Non-volatile
  - High density
  - Non-destructive read
  - Low V and P
  - ~10^{12} write/erase cycles
  - Easy to integrate

The Future

- Continue CMOS nanoscaling
- Non-classical CMOS
- Convergence
- Novel devices

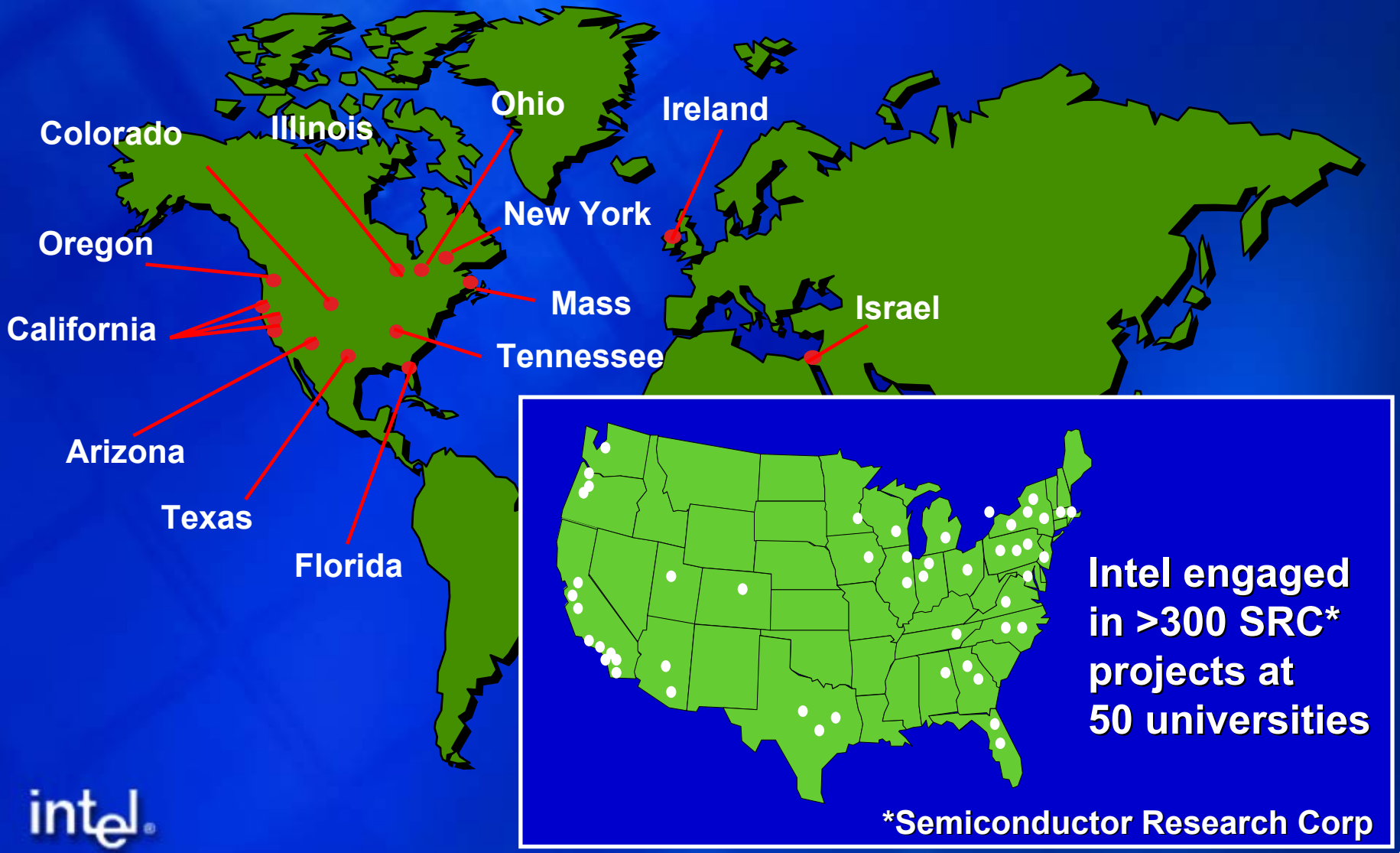
Novel Devices: R+D Time Requirements

- Product development spectrum
  - Software
  - System
  - Assembly
  - μArch
  - Power delivery and cooling
  - Circuit Design
  - Layout
  - Processing
  - Materials
- Change that affects one level or two adjacent levels is relatively easy to manage → 2-5 years R+D effort
- Change that affects many levels is very difficult → 6 – 20 years R+D effort
  - Must coordinate all changes
  - Long lead times

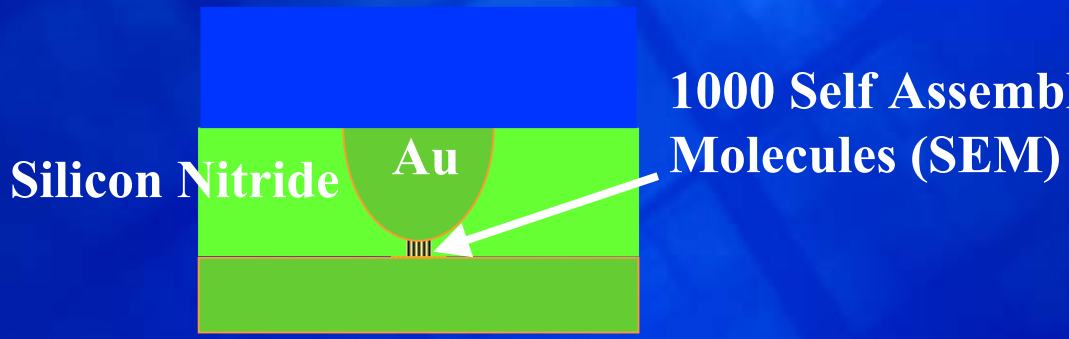
intel

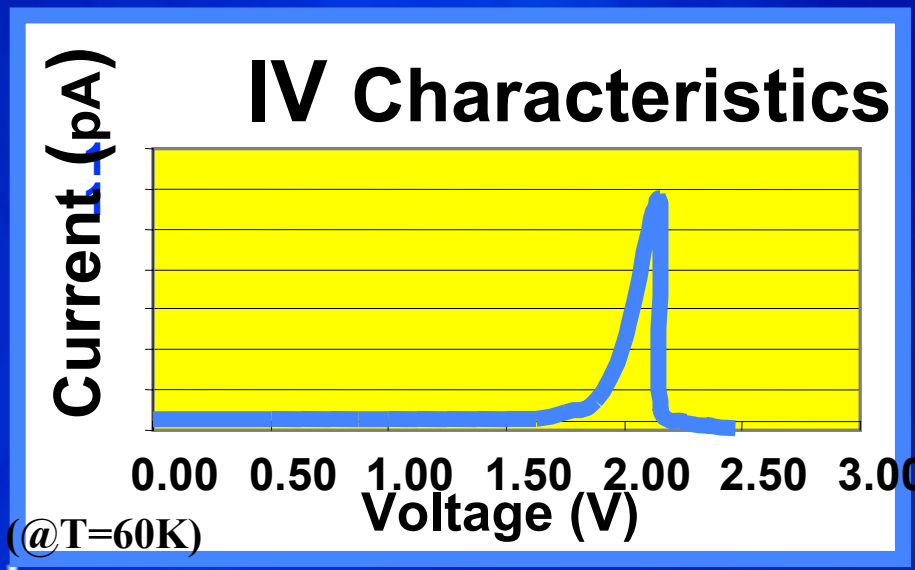
Intel and University Research

Intel-supported Nanotechnology Research at Universities



A Molecular Electronic Switch
(2-amino-4-ethyinylphenyl-4-ethylphenyl-5-nitro-1-benzenethiolate)

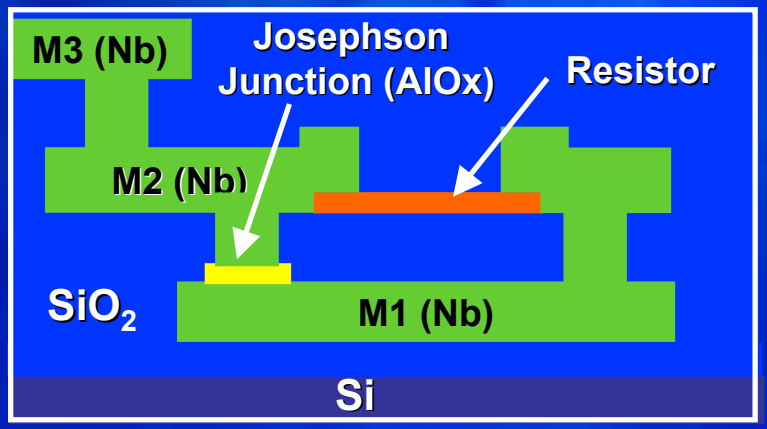


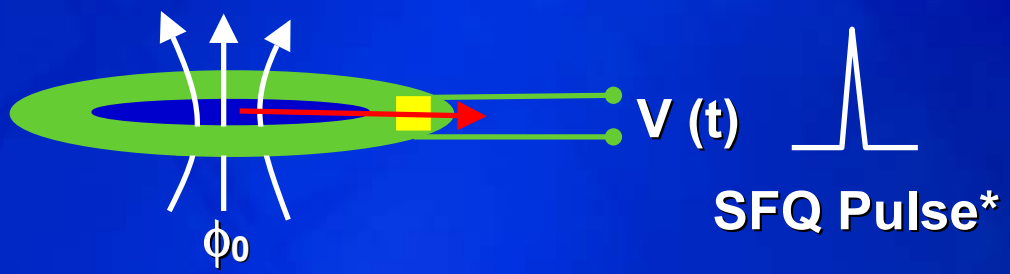


Source: M.Reed & others,Yale Univ and Rice Univ

- **Operation**
  - Applied voltage reconfigures molecules
  - Results in changed electrical properties
- **Attributes**
  - \+ Size (down to sub nm)
  - ? Interconnect
  - \- Kilohertz switching
  - \- No gain
  - \- Low current
  - \- Temperature stability
  - \- Large change across product spectrum

Rapid Single Flux Quantum Device





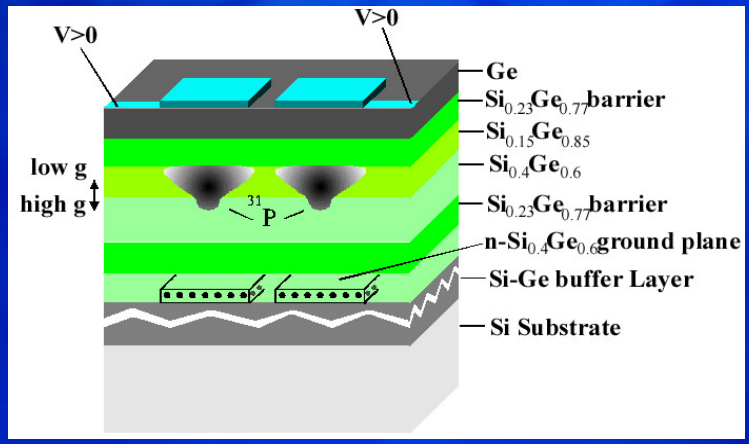
SFQ Pulse*

* $\int V(t)\,dt = \phi_0 = eh/c = 2$ mV-ps

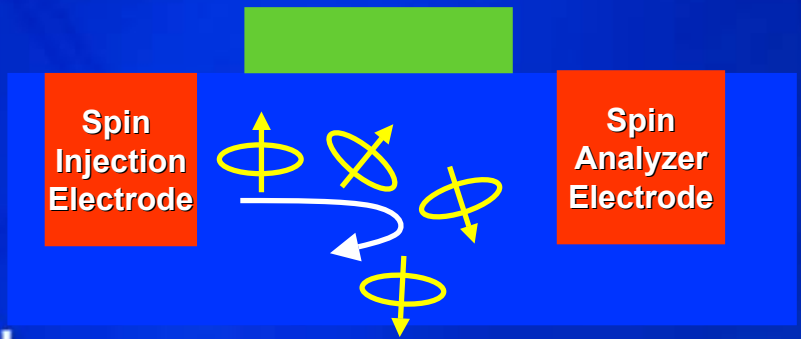
- **Operation**
  - Flux quanta (current loop) + Josephson Junction
  - JJ closed, emits stored flux quanta.
  - Quantized voltage pulse propagates down superconducting transmission line
- **Attributes**
  - \+ >>100GHz circuits
  - \+ Complex circuits demonstrated
  - \+ Very low power
  - \- ~5°K Operating Temp
  - \- High cost
  - \- > 100nm minimum feature size
  - \- Large change across product spectrum to implement

intel

Spin Resonance Transistor and Spintronics



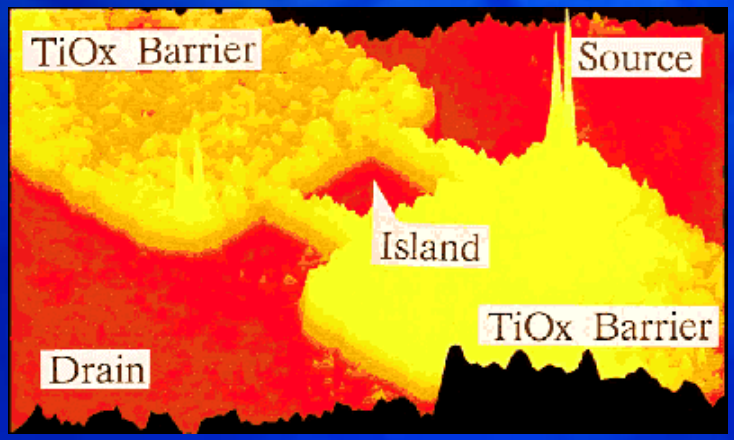
Courtesy Eli Yablanovitch, UCLA



- **Operation**
  - Transistors that respond to electron spin in addition to, or in lieu of electric charge.
  - Can conceive of configurations for optical isolators, magnetic sensors, NVM, FET and quantum devices.

- **Attributes**
  - \+ More energy efficient than conventional transistors
  - \+ Some configurations enable quantum computing
  - \+ Some configurations provide gain
  - \- Significant material development, spin injection and integration issues
  - \- Still at basic science level
  - \- Large change across product spectrum to implement

Room temperature Single Electron Transistor (SET)

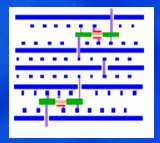
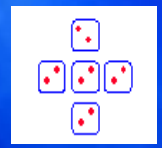
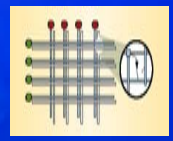
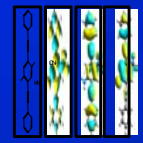
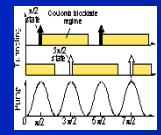
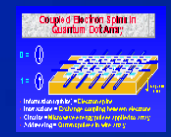


Courtesy, NEC, IEDM 2000, PP 481

- **Operation**
  - Single electron in "island" controls current flow from source to drain
  - Limited number of electron states in island
  - Electrons tunnel through barrier when S/D voltage is sufficient to overcome electrostatic repulsion in island

- **Attributes**
  - \+ Similar processing to Si CMOS
  - \+ Low power
  - \+ Gain
  - \- Low temp operation , or small feature size required
  - \- Low current drive
  - \- Very sensitive to misc charge
  - \- Large change across product spectrum to implement

Emerging Research Architectures

						
Architecture	3-D Integration	Quantum Cellular Automata	Defect Tolerant Architecture	Molecular Architecture	Cellular Nonlinear Networks	Quantum Computing
Device Implementation	CMOS with dissimilar material systems	Arrays of quantum dots	Intelligently assembles nanodevices	Molecular switches and memories	Single electron array architectures	Spin resonance transistors, NMR devices, Single flux quantum devices
Advantages	Less interconnect delay, Enables mixed technology solutions	High functional density. No interconnects in signal path	Supports hardware with defect densities >50%	Supports memory based computing	Enables utilization of single electron devices at room temperature	Exponential performance scaling, Enables unbreakable cryptography
Challenges	Heat removal, No design tools, Difficult test and measurement	Limited fan out, Dimensional control (low temperature operation), Sensitive to background charge	Requires pre-computing test	Limited functionality	Subject to background noise, Tight tolerances	Extreme application limitation, Extreme technology
Maturity	Demonstration	Demonstration	Demonstration	Concept	Demonstration	Concept

~2009? ← 2015++ →

Nanotechnology State Variables

- Electric charge
- Molecular state
- Spin orientation
- Electric dipole orientation
- Photon intensity
- Photon polarization
- Quantum state
- Phase state
- Mechanical state

Many Degrees Of Freedom For Nanodevices → Many Options

intel

Technical criteria

- *CMOS compatibility*
- *Energy efficiency*
- *Scalability*
- *Performance*
- *Architectural compatibility*
- *Sensitivity to parametric variation*
- *Room temperature operation*
- *Stability and reliability*

Option Must Be Superior to Si CMOS Based On Cost, Power, Performance

intel

The Ultimate Vision

The brain is the ultimate model for its ability to deal with complexity

- Little understanding on its architecture & organization
- Compared to tomorrow's computers
  - Orders of magnitude more powerful
  - Self assembled
  - Parallel operation
  - Self repairing to a significant degree
  - Fault tolerant
  - Runs on ~ 10W
  - 3D

Summary

- Nanotechnology is here today in "state of the art" high speed Si CMOS process technologies
- Si nanotechnology process scaling/convergence will continue for the next 10-15 years
- Alternative new technologies have emerged and will begin to be integrated into Si CMOS by 2015
- Nanoscience research is needed to facilitate these radical new scalable technologies beyond 2020

intel